EEL 4783: HDL in Digital System Design

Course:

Spring 2016. 3 credits.
Lectures: TTH 4:30-5:45PM @ HEC-0103
Instructor Office Hours: TTH 10:00AM~1:30PM and 2:45PM-4:30PM @ HEC 416

Course Instructor:

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Course Description:

This course provides a systematic introduction to the topic of HDL programming for designing embedded digital system. It emphasizes the basic ideas, and the practical aspects of HDL programming with FPGA devices. In addition, this course presents techniques for modeling hardware components at different levels of abstraction and many concepts including the various forms of expressing computations, sequential and parallel implementations, control-flow and data-flow, control dependency and data dependency, latency and throughput as well as the architecture design space of hardware data paths, finite state machines. Specific topics include:

- Basic concepts of HDL
- Veilog language and its usage.
- How to use Verilog to design large-scale and complicated digital systems.
- Identifying performance bottlenecks in a given hardware architecture and optimize it by transformations on hardware components
- How to use logic simulation to analyze and verity a HDL design.

Prerequisites:

EEL 3342: Digital Logic Design

Minimally Required Skills:

Basic logic design and basic software programming skills.

Recommended Text:

"Advanced Digital Design with the Verilog HDL" (2nd Edition) Hardcover – January 31, 2010 by Michael D. Ciletti

Grading:

The distribution of weights for the exams, assignments, and projects is as follows:

Midterm Exam	30%
Final Exam	20%
Final Project	25%
Assignments	25%

Students are encouraged to participate in class.

Honor System Policy:

Consultation with fellow students is encouraged, especially on design issues. However, directly copying another student's work defeats the purpose of the assignments and is an honor code violation. All written assignments should be original work. Portions of written work that are taken word-for-word from other authors (students or researchers) will be assigned a failing grade and may result in a failing grade in the course

Schedule (minor changes possible throughout the semester)

Event	Spring 2015	Topics	Notes	Assignments
Lecture 1		Introduction (Objectives, Expectations, Logistics)	pdf	
Lecture 2			pdf	
Lecture 3		Logic Design with Behavioral Models	pdf	
Lecture 4		Logic Design with Behavioral Models (cont.)	pdf	HW1, Solutions
Lecture 5		More Complex Behavioral Models	pdf	
Lecture 6		More Examples	pdf	HW2, Solutions
Lecture 7		Logic Synthesis	pdf	
Lecture 8		Logic Synthesis (cont.)	pdf	HW3, posted on webcourse
Lecture 9		Latch Synthesis	pdf	HW4, Solutions
Lecture 10		Flip-Flop Synthesis	pdf	
Lecture 11		Sequential Logic in Verilog	pdf	
Lecture 12		Revisit Sequential Logic	pdf	
Lecture 13		Midterm Review	1, 2	
Lecture 14		CORDIC Algorithm and Verilog Implementation	pdf	
Lecture 15		Logic Synthesis with Verilog	pdf	HW5 and solutions
Lecture 16		Floating Number	pdf	
Lecture 17		Microprocessor Design and inpolementation	pdf	midterm solutions
Lecture 18		Generate	pdf	
Lecture 19		Arith. Modules	pdf	

Lecture 20		Logic Verification	pdf	
Lecture 21		Verilog vs. VHDL	pdf	
		Final Review	pdf	

Final Exam		Thursday, April 28, 2016 4:00 PM – 6:50 PM		

Sample midterm 1, sols

Sample Midterm 2

Sample Final
Solutions

Assignments and Projects:

1. Homework assignment will be weekly and programming project will be bi-weekly.

2. Final Project Files:

Project 1. CORDIC Implementation

Project 2. 8-Bit CPU