EEL 4783: HDL in Digital System Design

Course:

Spring 2015. 3 credits.
Lectures: TTH 4:30-5:45PM @ ENG2-302
Instructor Office Hours: TTH 10:00AM~1:30PM and 2:45PM-4:30PM @ HEC 416

Course Instructor:

Mingjie Lin
Office: HEC 416, Telephone: 407-882-2298
Email: mingjie@eecs.ucf.edu, Home Page: http://www.eecs.ucf.edu/~mingjie

TA: aljobory3000@yahoo.com

Course Description:

This course provides a systematic introduction to the topic of HDL programming for designing embedded digital system. It emphasizes the basic ideas, and the practical aspects of HDL programming with FPGA devices. In addition, this course presents techniques for modeling hardware components at different levels of abstraction and many concepts including the various forms of expressing computations, sequential and parallel implementations, control-flow and data-flow, control dependency and data dependency, latency and throughput as well as the architecture design space of hardware data paths, finite state machines. Specific topics include:

- Basic concepts of HDL
- Veilog language and its usage.
- How to use Verilog to design large-scale and complicated digital systems.
- Identifying performance bottlenecks in a given hardware architecture and optimize it by transformations on hardware components
- How to use logic simulation to analyze and verity a HDL design.

Prerequisites:

EEL 3342: Digital Logic Design

Minimally Required Skills:

Basic logic design and basic software programming skills.

Recommended Text:

"Advanced Digital Design with the Verilog HDL" (2nd Edition) Hardcover – January 31, 2010 by Michael D. Ciletti

Grading:

The distribution of weights for the exams, assignments, and projects is as follows:

Midterm Exam	30%
Final Exam	20%
Final Project	25%

Assignments	25%

Students are encouraged to participate in class.

Honor System Policy:

Consultation with fellow students is encouraged, especially on design issues. However, directly copying another student's work defeats the purpose of the assignments and is an honor code violation. All written assignments should be original work. Portions of written work that are taken word-for-word from other authors (students or researchers) will be assigned a failing grade and may result in a failing grade in the course

Schedule (minor changes possible throughout the semester)

Event	Spring 2015	Topics	Notes	Assignments
Lecture 1	Jan 13	Introduction (Objectives, Expectations, Logistics)	pdf	
Lecture 2	Jan 15		pdf	
Lecture 3	Jan 20	Logic Design with Behavioral Models	pdf	
Lecture 4	Jan 22	Logic Design with Behavioral Models (cont.)	pdf	HW1 (Due Jan 29)
Lecture 5	Jan 27	More Complex Behavioral Models	pdf	Tutorial
Lecture 6	Jan 28	More Examples	pdf	1. HW1-sol 2. HW2 (Due Feb 5) (use webcourse to submit only)
Lecture 7	Feb. 2	Logic Synthesis	pdf	
Lecture 8	Feb. 5	Logic Synthesis (cont.)	pdf	1. HW2-sol 2. HW3 (Due Feb 12) (use webcourse to submit only) Finish 2 verilog programs: 1. addsub.v 2. shifter.v Solutions: 1. addsub.v 2. shifter.v
Lecture 9	Feb. 10	Latch Synthesis	pdf	
				1. HW4 (Due Feb 19 in

Lecture 10	Feb. 12	Flip-Flop Synthesis	pdf	class) (Paper Submission), HW4 Solutions.
Review I	Feb. 17	Midterm Review I	pdf	
Review II	Feb. 19	Midterm Review II	pdf	
	Feb, 24	Midterm Study (No Class)		Sample Midtem I and Solutions
	Feb. 26	Midterm I (in class, one hour)		
Lccture 11	March 3	Revisit Sequnetial Logic Design	pdf	1. HW5 is out, due on March 19.
Lecture 12	March 24	Real-World Design Problems	pdf	HW5 Due today. HW5 Solutions.
Lecture 13	March 31	Fun with FlipFlops	pdf	

Final Exam		TBD		

Assignments and Projects:

1. Homework assignment will be weekly and programming project will be bi-weekly.

2. Final Project Files:

Processor example slides

Assignment

file1
file2
file3

We supply the memory map in this file.